

Application Serial No. 10/611,307
Responsive to the Office Action Mailed: September 13, 2007

REMARKS

This Amendment is in response to the Office Action mailed on December 13, 2007.
Claim 15 is amended editorially. No new matter is added. Claims 15-18 are pending.

Status of Claims and Statement of Support for Claim Changes - 37 CFR 1.173(c):

Claim 1-14: cancelled.

Claim 15: pending. Claim 15 is amended and is supported, for example, in the specification in Figures 2, 6, 8, 10 and 15.

Claims 16-18: pending. Not amended.

PTO '892 Form:

Please note that Jones (US Patent No. 5,696,394) and Iwasa (US Patent No. 5,361,234), used in the §103 rejection of the present Office Action are not listed in a PTO '892 form. Applicants respectfully request that these references be listed on a PTO '892 form with the response to this Amendment.

§103 Rejections:

Claims 15-18 are rejected as being unpatentable over Jones in view of Iwasa. This rejection is traversed.

Claim 15 is directed to a semiconductor device that requires, among other features, a plurality of semiconductor elements and a plurality of dummy semiconductor elements. Claim 1 also requires a semiconductor element area on a substrate, which includes the plurality of semiconductor elements, the semiconductor element area being surrounded by the plurality of dummy semiconductor elements. Also, each of the plurality of semiconductor elements and each of the plurality of dummy semiconductor elements have the same dimensions. An advantage of requiring each of the plurality of semiconductor elements to have the same dimensions as each of the plurality of dummy semiconductor elements is to prevent deterioration of a crystalline structure of the ferroelectric material layer at the outermost position of the semiconductor element area during a process of etching the top electrode.

The combination of Jones and Iwasa does not teach or suggest these features. The rejection asserts that Iwasa teaches the feature of a plurality of dummy semiconductor elements.

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However, nowhere does Iwasa suggest that each of the plurality of semiconductor elements and each of the plurality of dummy semiconductor elements have the same dimensions. Iwasa is directed to a semiconductor memory device in which dummy memory cells are arranged at an adjacent portion to a boundary area between a memory cell array area and a peripheral circuit area so as to reduce a level difference between the memory cell array area and the peripheral circuit area (see column 6, line 1-column 7, line 34). However, the stacked capacitor electrode 106 has different dimensions than the dummy capacitor electrode 106d and thus the memory cells of Iwasa do not have the same dimensions of the dummy memory cells, as required by the semiconductor elements and the dummy semiconductor elements of claim 15. Jones does not overcome these deficiencies as Jones does not include dummy semiconductor elements.

Also, there is no suggestion in Jones or Iwasa to modify the dummy memory cells in Iwasa to have the same dimensions as the memory cells. As disclosed above, by requiring each of the plurality of semiconductor elements to have the same dimensions as each of the plurality of dummy semiconductor elements, deterioration of a crystalline structure of the ferroelectric material layer at the outermost position of the semiconductor element area during a process of etching the top electrode is prevented. In contrast, Iwasa is directed to a DRAM semiconductor device and therefore is not concerned with preventing a deterioration of a crystalline structure of a ferroelectric material layer. As discussed above, Jones does not include dummy semiconductor elements and therefore does not provide any suggestion for providing dummy semiconductor elements with the same dimensions as the semiconductor elements. For at least these reasons claim 15 is not suggested by the combination of Jones and Iwasa. Claims 16-18 depend from claim 15 and should be allowed for at least the same reasons.

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Conclusion:

Applicants respectfully assert that claims 15-18 are in condition for allowance. If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' primary attorney-of record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.



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Respectfully submitted,

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